

What is claimed is:

1 1. A method of fabricating a polysilicon line, comprising:
2 forming a patterned hard mask layer over a polysilicon
3 layer;
4 patterning the polysilicon layer to provide a hard
5 mask-capped polysilicon line having a first width; and
6 isotropically removing portions of said polysilicon
7 line to a second width.

1 2. The method of claim 1, wherein said second width is sub-
2 minimum groundrule.

1 3. The method of claim 1, further including removing said
2 patterned hard mask layer

1 4. The method of claim 1, wherein said patterned hard mask
2 layer comprises silicon oxide.

1 5. The method of claim 1, wherein isotropically removing
2 portions of said polysilicon line comprises converting a

3 surface layer of said polysilicon line to an oxide layer and
4 isotropically etching said oxide layer.

1 6. The method of claim 1, wherein the step of removing
2 portions of the polysilicon line comprises a treatment in a
3 saturated aqueous solution of O_3 followed by etching in a
4 solution comprising 1 part 49% HF in 50 to 300 parts of
5 water.

1 7. The method of claim 1, wherein the step of removing
2 portions of the polysilicon line comprises a treatment in a
3 saturated aqueous solution of O_3 followed by etching in an
4 HF containing vapor.

1 8. The method of claim 1, wherein the step of removing
2 portions of the polysilicon line comprises etching in a
3 solution of 1 part 49% HF, 100 to 200 parts 69% HNO_3 and 100
4 to 200 parts 85% H_3PO_4 .

1 9. The method of claim 1, wherein the step of removing
2 portions of the polysilicon line comprises etching in a

3 solution of 1.3 parts 30% NH_4OH , 3.1 parts 31% H_2O_2 and 80 to
4 100 parts of water.

1 10. A method of reducing transistor gate dimensions,
2 comprising:

3 forming a patterned hard mask layer over a polysilicon
4 layer, said polysilicon layer formed over a gate dielectric
5 layer;

6 patterning the polysilicon to provide a hard mask-
7 capped polysilicon electrode having a first width; and

8 isotropically removing portions of the polysilicon
9 electrode to a second width.

1 11. The method of claim 10, wherein said second width is
2 sub-minimum groundrule.

1 12. The method of claim 10, further including removing said
2 patterned hard mask layer.

1 13. The method of claim 10, wherein said patterned hard mask
2 layer comprises silicon oxide.

1 14. The method of claim 10, wherein isotropically removing
2 portions of said polysilicon electrode comprises converting

3 a surface layer of said polysilicon line to an oxide layer
4 and isotropically etching said oxide layer.

1 15. The method of claim 10, wherein the step of removing
2 portions of the polysilicon electrode comprises a treatment
3 in a saturated aqueous solution of O_3 followed by etching in
4 a solution comprising 1 part 49% HF in 50 to 300 parts of
5 water.

1 16. The method of claim 10, wherein the step of removing
2 portions of the polysilicon electrode comprises a treatment
3 in a saturated aqueous solution of O_3 followed by etching in
4 an HF containing vapor.

1 17. The method of claim 10, wherein the step of removing
2 portions of the polysilicon electrode comprises etching in a
3 solution of 1 part 49% HF, 100 to 200 parts 69% HNO_3 and 100
4 to 200 parts of 85% H_3PO_4 .

1 18. The method of claim 10, wherein the step of removing
2 portions of the polysilicon electrode comprises etching in a

3 solution of 1.3 parts 30% NH_4OH , 3.1 parts 31% H_2O_2 and 80 to
4 100 parts of water.

1 19. A method of forming a transistor gate, comprising:
2 forming a dielectric layer on a top surface of a
3 substrate;
4 forming a polysilicon layer on a top surface of said
5 dielectric layer;
6 forming a patterned hard mask layer on a top surface of
7 said polysilicon layer;
8 patterning the polysilicon to provide a hard mask-
9 capped polysilicon electrode having a first width; and
10 isotropically removing portions of the polysilicon
11 electrode to a second width.

1 20. The method of claim 19, wherein said second width is
2 sub-minimum groundrule.

1 21. The method of claim 19, further including removing said
2 patterned hard mask layer.

1 22. The method of claim 19, further including simultaneously
2 removing portions of said dielectric layer not covered by
3 said polysilicon gate electrode and said patterned hard
4 mask.

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1 23. The method of claim 19, wherein said hard mask layer and
2 said dielectric layer comprise silicon oxide.

1 24. The method of claim 19, wherein said substrate is
2 selected from the group consisting of silicon, silicon on
3 insulator, gallium arsenide and sapphire.

1 25. The method of claim 19, wherein the step of removing
2 portions of the polysilicon electrode comprises a treatment
3 in a saturated aqueous solution of O_3 followed by etching in
4 a solution comprising 1 part 49% HF in 50 to 300 parts of
5 water.

1 26. The method of claim 19, wherein the step of removing
2 portions of the polysilicon electrode comprises a treatment
3 in a saturated aqueous solution of O_3 followed by etching in
4 an HF containing vapor.

1 27. The method of claim 19, wherein the step of removing
2 portions of the polysilicon electrode comprises etching in a
3 solution of 1 part 49% HF, 100 to 200 part 69% HNO_3 and 100
4 to 200 parts of H_3PO_4 .

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1 28. The method of claim 19, wherein the step of removing
2 portions of the polysilicon electrode comprises etching in a
3 solution of 1.3 parts 30% NH_4OH , 3.1 parts 31% H_2O_2 and 80 to
4 100 parts of water.

1 29. A method of forming a transistor gate, comprising:
2 forming a dielectric layer on a top surface of a
3 substrate;
4 forming a polysilicon layer on a top surface of said
5 dielectric layer;
6 forming a patterned hard mask layer on a top surface of
7 said polysilicon layer;
8 patterning the polysilicon to provide a hard mask-
9 capped polysilicon electrode having a first width;
10 measuring said first width;
11 comparing said first width to a target width and
12 determining a delta;
13 calculating an etch time or a number of polysilicon
14 oxidation/isotropic polysilicon etch cycles based on said
15 delta; and
16 performing an isotropic polysilicon etch for the
17 calculated time or performing the calculated number of
18 polysilicon oxidation/isotropic polysilicon etch cycles.

1 30. The method of claim 29, wherein said target width is
2 sub-minimum groundrule.

1 31. The method of claim 29, further including removing said
2 patterned hard mask layer.

1 32. The method of claim 29, further including simultaneously
2 removing portions of said dielectric layer not covered by
3 said polysilicon gate electrode and said patterned hard
4 mask.

1 33. The method of claim 29, wherein said hard mask layer and
2 said dielectric layer comprise silicon oxide.

1 34. The method of claim 29, wherein said substrate is
2 selected from the group consisting of silicon, silicon on
3 insulator, gallium arsenide and sapphire.

1 35. A polysilicon line fabricated by the process comprising:
2 forming a patterned hard mask layer over a polysilicon
3 layer;
4 patterning the polysilicon to provide a hard mask-
5 capped polysilicon line having a first width; and
6 isotropically removing portions of said polysilicon
7 line to a second width.

1 36. The polysilicon line of claim 35, wherein said second
2 width is sub-minimum groundrule.

1 37. The polysilicon line of claim 35, wherein said substrate
2 is selected from the group consisting of silicon, silicon on
3 insulator, gallium arsenide and sapphire.

1 38. A polysilicon transistor gate fabricated by the process
2 comprising:

3 forming a patterned hard mask layer over a polysilicon
4 layer, said polysilicon layer formed over a gate dielectric
5 layer;

6 patterning the polysilicon to provide a hard mask-
7 capped polysilicon electrode having a first width;

8 isotropically removing portions of said polysilicon
9 electrode to a second width; and

10 removing said patterned hard mask layer.

1 39. The polysilicon transistor gate of claim 38, wherein
2 said second width is sub-minimum groundrule.

1 40. The polysilicon transistor gate of claim 39, wherein
2 said substrate is selected from the group consisting of
3 silicon, silicon on insulator, gallium arsenide and
4 sapphire.

1 41. A polysilicon transistor gate fabricated by the process
2 comprising:

3 forming a dielectric layer on a top surface of a
4 substrate;

5 forming a polysilicon layer on a top surface of said
6 dielectric layer;

7 forming a patterned hard mask layer on a top surface of
8 said polysilicon layer;

9 patterning the polysilicon to provide a hard mask-
10 capped polysilicon electrode having a first width;

11 isotropically removing portions of said polysilicon
12 electrode to a second width; and

13 removing said patterned hard mask layer.

1 42. The polysilicon transistor gate of claim 41, wherein
2 said second width is sub-minimum groundrule.

1 43. The polysilicon transistor gate of claim 41, wherein
2 said substrate is selected from the group consisting of
3 silicon, silicon on insulator, gallium arsenide and
4 sapphire.